145 Adams Avenue, Hauppauge, NY 11788, USA
Tel: 1.631.435.1110 Fax: 1.631.435.1824
www.centralsemi.com
mailto:processchange@centralsemi.com
https://www.centralsemi.com/process-change-notices

PCN # 236
Notification Date: October 4, 2022

Product / Process Change Notice

Devices affected:
The following P-Channel JFETs:

Part numbers affected:

TO-92 Case	TO-18 Case	TO-72 Case
2N5460	2N2608	2N3330
2N5461		
2N5462		
2N3820		
PN5033		

Extent of change:
Change in wafer fab, resulting in change in die size from 20 x 20 mils to 18.9 x 18.9 mils (see Table 1).

Reason for change:
As part of Central Semiconductor's supply chain risk mitigation initiative, and in an effort to ensure an undisrupted supply of product, a change in wafer fabrication site is being made for the products referenced above. Product specifications, quality and reliability are not impacted by this change.

Effect of change:
This change does not affect the fit, form or function of the devices.

Earliest effective date of change:
October 4, 2022

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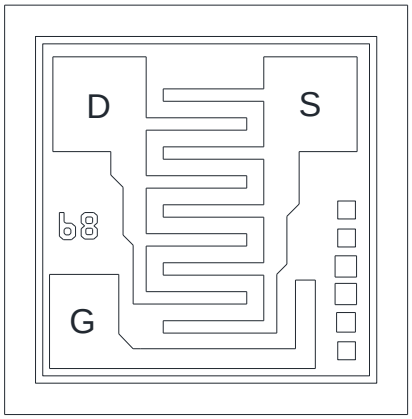
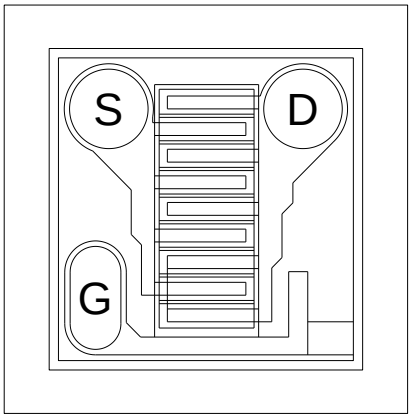
Table 1:

Before Change



Die Size	20 x 20 MILS
Die Thickness	8.0 MILS
Drain Bonding Pad Size	4.0 x 4.0 MILS
Source Bonding Pad Size	4.0 x 4.0 MILS
Gate Bonding Pad Size	3.0 x 4.0 MILS
Top Side Metalization	Al – 30,000Å
Back Side Metalization	Au – 6,000Å

After Change



Die Size	18.9 x 18.9 MILS
Die Thickness	7.9 MILS
Drain Bonding Pad Size	4.2 MILS DIAMETER
Source Bonding Pad Size	4.2 MILS DIAMETER
Gate Bonding Pad Size	2.9 x 5.3 MILS
Top Side Metalization	Al-Si – 17,000Å
Back Side Metalization	Au – 12,000Å

Qualification data:

Test	Condition	Failure rate
High Temperature Storage Life/ bake test.	150°C (-0/+10)°C, 1000 hours. **JESD22-A103**	0/77
Temperature Cycling	T= -65°C to +150°C 1000 cycles. Dwell time = 15 min. **JESD22-A104 & MIL-STD-750 TM1051**	0/77
High Temperature Gate Bias (HTGB)	T=125°C, t=1000 hours, Bias at V_GS from gate to source with source and drain shorted **JESD22-A108**	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)	T = 110°C, RH = 85%, and t = 264 hours. Bias conditions per device specification sheet. **JESD22-A110**	0/77

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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	