

Product / Process Change Notice

Parts Affected:

Chip process CP206, N-Channel Field Effect Transistors, wafers, and bare die.

Extent of Change:

The CP206 wafer process has been discontinued and replaced with the CP216 wafer process. See figures 1 and 2 for details.

Reason for Change:

This process was transferred to an alternate wafer foundry which provides improved and consistent yields.

Revision 1 September 26, 2019: Issued to include additional devices not on the initial PCN release. Newly added devices are shown in the “Part Numbers Affected” section on page 3 marked with *.

Effect of Change:

The wafer process meets all electrical specifications of the individual devices listed on the following page.

Qualification:

Test	Condition	Failure rate
Resistance to Solder Shock	T = 260°C ± 5°C Dwell time = 10 sec. JESD22-B106	0/77
High Temperature Storage Life/ bake test.	150°C (-0/+10)°C, 1000 hours. JESD22-A103	0/77
Temperature Cycling	T = -65°C to +150°C 1000 cycles. Dwell time = 15 min. JESD22-A104	0/77
High Temperature Reverse Bias (HTRB)	T = 125°C, t = 1000 hours, V _R = V _Z JESD22-A108	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)	T = 130°C, RH = 85%, P = 33.3 psia, and t = 96 hours. Bias conditions per device specification sheet. JESD22-A110	0/77
Accelerated Moisture Resistance Unbiased Autoclave	Temperature = 121°C ± 2°C; relative humidity = 100%; vapor pressure = 29.7 psia (15psig). t = 96 hours JESD22-A102	0/77

Effective Date of Change:

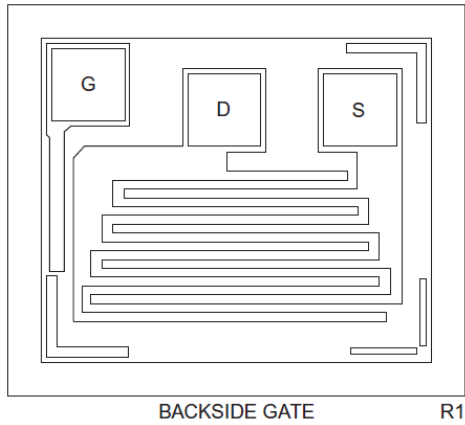
April 16, 2018 - Existing inventory will be shipped until depleted.

PCN # 165_Rev 1
Revision Notification Date: 26 Sept. 2019
Original Notification Date: 16 April 2018

Sample Availability:

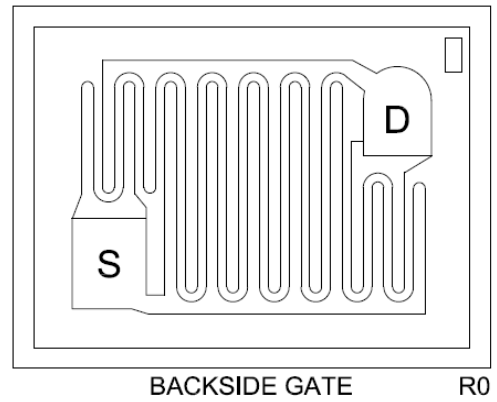
Please contact Salesperson or Manufacturer's Representative.

Figure 1: CP206 Chip Geometry (Discontinued)



Wafer Diameter:	5 inch
Die Size:	21 x 18 mils
Die Thickness:	8.0 mils
Bond Pad Size (Drain):	3.0 x 3.0 mils
Bond Pad Size (Source):	3.0 x 3.0 mils
Bond Pad Size (Gate):	3.0 x 3.0 mils
Topside Metal:	Al (30,000Å)
Backside Metal:	Au (6,000Å)

Figure 2: CP216 Chip Geometry



Wafer Diameter:	4 inch
Die Size:	21 x 16 mils
Die Thickness:	7.9 mils
Bond Pad Size (Drain):	3.3 x 4.5 mils
Bond Pad Size (Source):	3.3 x 4.5 mils
Topside Metal:	Al (10,000Å)
Backside Metal:	Au (3,250Å)

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Part Numbers Affected:

2N4391	CP206-2N4391-CT
2N4392	CP206-2N4391-WN
2N4393	CP206-2N4392-CM
2N4092	CP206-2N4392-CT
2N4861	CP206-2N4392-WN
2N4861A	CP206-2N4393-CT
CMPF4391	CP206-2N4393-WN
CMPF4392	CP206-2N4856-CM*
CMPF4393	CP206-2N4856-CT*
PN4091*	CP206-2N4856-WN*
PN4092*	2N4091*
PN4093*	2N4856*
PN4391*	2N4856A*
PN4392*	2N4857*
PN4393*	2N4857A*
CEN1280*	2N4859*
	2N4859A*

*Revision 1 September 26, 2019 newly added devices



145 Adams Avenue, Hauppauge, NY 11788 USA
Tel: (631) 435-1110 • Fax: (631) 435-1824
www.centralsemi.com
<mailto:processchange@centralsemi.com>
<http://www.centralsemi.com/processchange>

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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	