

## Product / Process Change Notice

**Parts Affected:**

Chip process CP319, NPN silicon power transistors, wafers, and bare die.

**Extent of Change:**

The CP319 wafer process has been discontinued and replaced with the CP212 wafer process. See figures 1 and 2 for details.

**Reason for Change:**

New wafer process provides an improved and consistent yield. Revision 1 of this PCN was released to include additional "Part Numbers Affected" on the following page that were not included in the initial PCN release.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Effective Date of Change:**

January 11, 2016

**Sample Availability:**

Please contact Salesperson or Manufacturer's Representative.

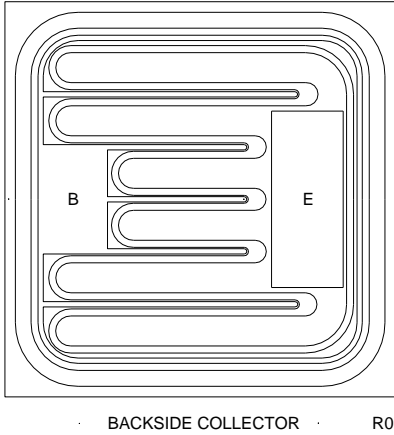
**Qualification Tests:**

Test	Condition	Failure rate
Resistance to Solder Shock	T = 260°C ± 5°C Dwell time = 10 sec. <b>JESD22-B106</b>	0/77
High Temperature Storage Life/ bake test.	Specified temperature (-0/+10)°C, 1000 hours. <b>JESD22-A103</b>	0/77
Temperature Cycling	T = -65°C to +150°C 1000 cycles. Dwell time = 15 min. <b>JESD22-A104</b>	0/77
High Temperature Reverse Bias (HTRB)	T = 125°C, t = 48 hours, 80% MAX rated VCB <b>JESD22-A108</b>	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)	T = 130°C, RH = 85%, P = 33.3 psia, and t = 96 hours. Bias conditions per device specification sheet. <b>JESD22-A110</b>	0/77
Accelerated Moisture Resistance Unbiased Autoclave	Temperature = 121°C ± 2°C; relative humidity = 100%; vapor pressure = 205kPa, 29.7 psia. t = 48 hours <b>JESD22-A102</b>	0/77

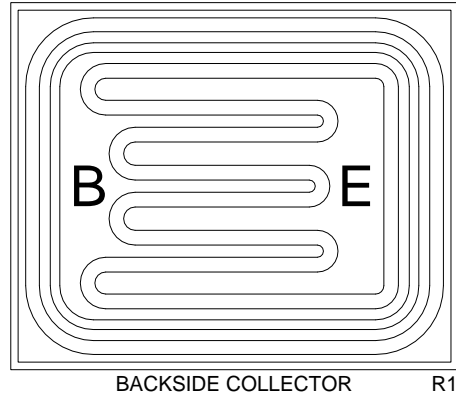
**Figures:**

**PCN #156 Revision 1**  
**Revision Notification Date: 3 March 2016**  
**Original Notification Date: 22 Dec 2015**

**Figure 1: CP319 Chip Geometry (Discontinued)**



**Figure 2: CP212 Chip Geometry**



Wafer Diameter: 4 inch  
Die Size: 87 x 87 mils  
Die Thickness: 9.0 mils  
Bond Pad Size (Emitter): 38 x 16 mils  
Bond Pad Size (Base): 24 x 15 mils  
Topside Metal: Al (30,000Å)  
Backside Metal: Ti/Ni/Ag (11,000Å)

Wafer Diameter: 4 inch  
Die Size: 80 x 99 mils  
Die Thickness: 12 mils  
Bond Pad Size (Emitter): 48 x 13 mils  
Bond Pad Size (Base): 32 x 12 mils  
Topside Metal: Al (30,000Å)  
Backside Metal: Cr/Ni/Ag (16,000Å)

**Part Numbers Affected:**

CJD47	2N5051
CJD50	2N5052
2N3583	CEN736
2N3584	CEN853
2N3585	CP319-CJD50-CT
2N3738	CP319-TIP47-CT
2N3739	CP319-TIP50-CT
2N4240	CP319-CZTA44HC-CT
2N4296	CP319-CZTA44HC-WN
2N4298	CP319-2N3585-WN
2N4299	CP319-2N4240-WN
2N5050	



145 Adams Avenue, Hauppauge, NY 11788 USA  
Tel: (631) 435-1110 • Fax: (631) 435-1824

[www.centralsemi.com](http://www.centralsemi.com)  
<mailto:processchange@centralsemi.com>  
<http://www.centralsemi.com/processchange>

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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	